Office of Science
U.S. DEPARTMENT OF ENERGY

Advanced Scientific Computing Research

The Potential of the Cell Processor for Scientific Computing (2006)

Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands,
and Katherine Yelick, Lawrence Berkeley National Laboratory

Publication of the paper "The Potential of the Cell Processor for Scientific Computing" was one of the most talked-about events of 2006 in the scientific computing community. The paper found that on average, Cell was eight times faster and at least eight times more power efficient than Opteron and Itanium processors in running several scientific application kernels. This paper helped pave the way for implementations of Cell-based systems at many scientific computing centers, including the current fastest computer in the world (Roadrunner) and the three most energy-efficient supercomputers.

Though it was designed as the heart of the Sony PlayStation3 game console, the STI Cell processor created quite a stir in the computational science community when it was introduced. The Cell processor's potential as a building block for high performance computers was a topic of widespread discussion and speculation.

To evaluate Cell's potential, computer scientists at Lawrence Berkeley National Laboratory evaluated the processor's performance in running several scientific application kernels, then compared this performance with other processor architectures. The results of the group's evaluation were presented in a paper at the ACM International Conference on Computing Frontiers, held May 2–6, 2006, in Ischia, Italy; reviewers ranked it highest among the conference paper submissions.

The paper, "The Potential of the Cell Processor for Scientific Computing," was written by Samuel Williams, Leonid Oliker, Parry Husbands, Shoaib Kamil and Katherine Yelick of Berkeley Lab's Computation Research Division and John Shalf of NERSC. (Yelick is now NERSC Director.)

"Overall results demonstrate the tremendous potential of the Cell architecture for scientific computations in terms of both raw performance and power efficiency," the authors wrote in their paper. "We also conclude that Cell's heterogeneous multi-core implementation is inherently better suited to the HPC environment than homogeneous commodity multicore processors."

Cell, designed by a partnership of Sony, Toshiba, and IBM, is a high performance implementation of software-controlled memory hierarchy in conjunction with the considerable floating point resources that are required for demanding numerical algorithms. Cell takes a radical departure from conventional multiprocessor or multi-core architectures. Instead of using identical cooperating commodity processors, it uses a conventional high performance PowerPC core that controls eight simple SIMD (single instruction, multiple data) cores, called synergistic processing elements (SPEs), where each SPE contains a synergistic processing unit (SPU), a local memory, and a memory flow controller (Figure 1).

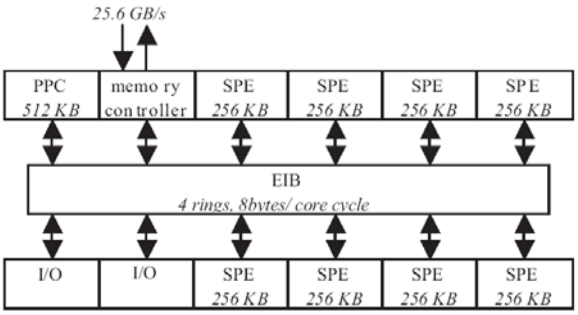

Figure 1. Overview of the Cell processor architecture.

Despite its radical departure from mainstream general-purpose processor design, Cell is particularly compelling because it is produced at such high volumes that it is cost-competitive with commodity CPUs. At the same time, the slowing pace of commodity microprocessor clock rates and increasing chip power demands have become a concern to computational scientists, encouraging the community to consider alternatives like STI Cell.

The authors examined the potential of using the STI Cell processor as a building block for high-end

parallel systems by investigating performance across several key scientific computing kernels: dense matrix multiply, sparse matrix vector multiply, stencil computations on regular grids, as well as 1D and 2D fast Fourier transformations.

According to the researchers, the then-current implementation of Cell was most often noted for its extremely high performance single-precision (32-bit) floating performance, but the majority of scientific applications require double precision (64-bit). Although Cell's peak double-precision performance was still impressive relative to its commodity peers (eight SPEs at 3.2 GHz = 14.6 Gflop/s), the group quantified how modest hardware changes could improve double-precision performance. (The subsequent PowerXCell 8i version superseded these modest double-precision performance enhancements.)

The authors developed a performance model for Cell and used it to show direct comparisons of Cell with the AMD Opteron, Intel Itanium2 and Cray X1 architectures. The performance model was then used to guide implementation development that was run on IBM's Full System Simulator in order to provide even more accurate performance estimates.

The authors argued that Cell's three-level memory architecture, which decouples main memory accesses from computation and is explicitly managed by the software, provides several advantages over mainstream cache-based architectures. First, performance is more predictable, because the transfer time between an SPE's local store and DRAM is easily predicted. Second, long block transfers from off-chip DRAM can achieve a much higher percentage of memory bandwidth than individual cache-line loads. Finally, for predictable memory access patterns, communication and computation can be effectively overlapped by careful scheduling in software.

"Overall results demonstrate the tremendous potential of the Cell architecture for scientific computations in terms of both raw performance and power efficiency," the authors wrote. While their analysis used hand-optimized code on a set of small scientific kernels, the results were striking. On average, Cell was eight times faster and at least eight times more power efficient than Opteron and Itanium processors, despite the fact that Cell's peak double-precision performance was, at that time, fourteen times slower than its peak single-precision performance.

This paper quickly became one of the most talked-about topics in the high performance computing community, with reports and commentaries in several publications. An article about this research in the May 26, 2006 issue of HPCwire became the most downloaded article in the online magazine's history.

By quantifying and validating the potential of the Cell processor for scientific computing, this paper helped pave the way for implementations of Cell-based systems at many scientific computing centers. These implementations include:

- The IBM Roadrunner system at Los Alamos National Laboratory, an Opteron- and Cell-based supercomputer, became the world's first system to achieve 1 petaflops performance in May 2008 and was ranked the fastest computer in the world on the June 2008 TOP500 List. Roadrunner uses the PowerXCell 8i version of the Cell processor, in which the SPUs have been enhanced to deliver 102 Gflop/s of double-precision performance per chip.

- The world's three most energy-efficient supercomputers, as represented on the June 2008 Green500 List, are based on the PowerXCell 8i.

- Clusters of PlayStation3 consoles are being used by several research groups. And with over half a million PlayStation3 consoles added to other home computers, the distributed computing project Folding@Home has been recognized by Guinness World Records as the most powerful distributed network in the world, achieving over 1 petaflops performance. Folding@Home seeks to analyze and understand protein folding, a little understood process that is fundamental to virtually all of biology.

Publications:

Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands, and Katherine Yelick, "The Potential of the Cell Processor for Scientific Computing," Proceedings of the 3rd Conference on Computing Frontiers, Ischia, Italy, 2006.

Samuel Williams, John Shalf, Leonid Oliker, Shoaib Kamil, Parry Husbands, and Katherine A. Yelick, "Scientific Computing Kernels on the Cell Processor," International Journal of Parallel Programming **35**, 263 (2007).

Funding:

DOE Office of Advanced Scientific Computing Research.